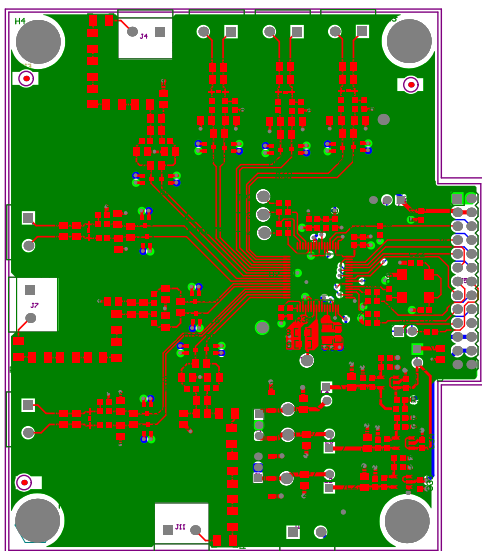


Layer Stack Up Detail for: TIDA-00661-B.PcbDoc			
Layer Name	Material	Copper Thickness	Soldermask Material
Top Solder Mask	C.0750		Solder Resist
Top Layer	C.07L3	1.4mil	FR4-High Tg
Core	C.051	1.4mil	FR4-High Tg
Ply	C.022	1.4mil	FR4-High Tg
Bottom Layer	C.08L3	1.4mil	FR4-High Tg
Bottom Solder Mask	C.0850		Solder Resist

Z21 ■ Install label in silkscreened box after final wash. Text shall be 8 pt font. Text shall be per the Label Table in the PDF schematic.
Z22 ■ These assemblies are ESD sensitive, ESD precautions shall be observed.
Z23 ■ These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.
Z24 ■ These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.



COMPONENTS MARKED "IMP" SHOULD NOT BE REPLACED.
ASSEMBLY REQUIREMENTS
(No Variations)

DESIGNED BY: TONY CLARK
CHECKED BY: TONY CLARK
DATE: 12/10/2015

ALL LAYERS VIEWED FROM TOP SIDE	BOARD #:	REV:	SWN REV:	NOTES
LAYER NAME = TOP	1000-00661-B	E2	1.0	1000-00661-B
Plot Name = 1000-00661-B_Top	GENERATED:	12/10/2015 10:23:34 AM	1000-00661-B	1000-00661-B

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PROJECT TITLE: TIDA-00661_ADC_Card	ENGINEER: Greenivasa kallikuppa
DESIGNED FOR: Public Release	LAYOUT BY: Avinash N
FILE NAME: TIDA-00661-B .PcbDoc	ALTIM DESIGNER VERSION: 14.3.14.34663
SCALE: 0.72	